ABSTRACT OF THE DISCLOSURE

An apparatus for performing an MMX PSADBW instruction is disclosed. The apparatus includes carry-generating subtraction logic that generates packed differences of the subtrahend from the minuend and associated carry bits indicating whether the difference is positive or negative. The apparatus selectively inverts the differences based on the carry bits. Addition logic adds the selectively inverted differences and carry bits substantially in parallel to generate the PSADBW instruction result. In one embodiment, the apparatus also includes two muxes. The first mux selects the selectively inverted differences in the case of a PSADBW instruction and selects a multiply instruction's partial products otherwise. The second mux selects the carry bits in the case of a PSADBW instruction and selects a second multiply instruction's partial products otherwise. The two mux outputs are provided to the addition logic. In one embodiment, the microprocessor translates the PSADBW instruction into at least first and second microinstructions for execution.